In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

1. (Currently Amended) A computer system comprising:

a central processing unit (CPU); and

a cache memory, coupled to the CPU, including:

a main cache having a plurality of cache lines, each of the plurality of cache lines being compressible to form compressed cache lines to store additional data; and

a plurality of storage pools to hold a segment of the additional data for a compressed cache line; and

a cache controller having compression logic to determine that a retrieved cache line is to be combined with a resident companion cache line to form the compressed cache line if the companion cache line is resident in the cache memory and to store the compressed cache line in the cache line of the resident companion ~~form the compressed cache line by combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having a second address comprising a second companion bit value if the companion cache line is resident in the cache memory, wherein the second address differs from the first address by the second companion bit~~.

2. (Original) The computer system of claim 1 wherein each of the plurality of storage pools include a plurality of fixed width storage fields.

3. (Original) The computer system of claim 1 wherein the plurality of cache lines are included within a plurality of sets.

4. (Original) The computer system of claim 3 wherein a storage pool is allocated to each of the plurality of sets.

5. (Original) The computer system of claim 4 wherein an indicator is associated with each storage field of a storage pool to indicate a line within one of the plurality of sets to which a storage field is assigned.

6. (Previously Presented) The computer system of claim 3 wherein multiple storage fields within each storage pool is allocated a line within one of the plurality of sets.

7. (Original) The computer system of claim 6 wherein each storage field mapped to one of the plurality of sets is sorted according to a logical ordering.

8. (Original) The computer system of claim 3 wherein a storage pool is shared by two or more of the plurality of sets.

9. (Original) The computer system of claim 8 wherein an indicator is associated with each line of a storage pool to indicate which of the plurality of sets to which a storage field is assigned.

10. (Original) The computer system of claim 1 further comprising a cache controller coupled to the cache memory.

11. (Original) The computer system of claim 10 wherein the cache controller accesses the cache lines and storage pools in parallel.

12. (Original) The computer system of claim 11 wherein accessing the cache lines and storage pools in parallel comprises the cache controller simultaneously dispatching set bits to the cache lines and storage pools.

13. (Previously Presented) The computer system of claim 10 wherein the cache controller accesses the cache lines and storage pools serially.

14. (Original) The computer system of claim 3 wherein a storage pool is shared by all of the plurality of sets.

15. (Currently Amended) A cache memory comprising:

main cache having a plurality of cache lines, each of the plurality of cache lines being compressible to form compressed cache lines to store additional data, wherein a cache line is ~~compressed~~ determined to be compressible if a companion cache line of a retrieved cache line is resident in the cache memory, and wherein

the retrieved cache line and the companion cache line are combined and stored in the cache line of the resident companion if the cache line is determined to be compressible ~~by combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having a second address comprising a second companion bit value if the companion cache line is resident in the cache memory, wherein the second address differs from the first address by the second companion bit~~; and

a plurality of storage pools to hold a segment of the additional data for a compressed cache line.

16. (Original) The cache memory of claim 15 wherein each of the plurality of storage pools include a plurality of fixed width storage fields.

17. (Original) The cache memory of claim 15 wherein the plurality of cache lines are included within a plurality of sets.

18. (Original) The cache memory of claim 17 wherein a storage pool is allocated to each of the plurality of sets.

19. (Original) The cache memory of claim 18 wherein an indicator is associated with each storage field of a storage pool to indicate a line within one of the plurality of sets to which a storage field is assigned.

20. (Original) The cache memory of claim 17 wherein multiple storage fields within each storage pool is allocated a line within one of the plurality of sets.

21. (Original) The cache memory of claim 17 wherein a storage pool is shared by two or more of the plurality of sets.

22. (Original) The cache memory of claim 21 wherein an indicator is associated with each line of a storage pool to indicate which of the plurality of sets to which a storage field is assigned.

23. (Original) The cache memory of claim 17 wherein a storage pool is shared by all of the plurality of sets.

24. (Currently Amended) A method comprising:

compressing one or more of a plurality of cache lines to form one or more compressed cache lines to store additional data by:

determining if a companion cache line of a retrieved cache line is resident in a cache memory, and wherein the retrieved cache line and the companion cache line are combined;

combining the retrieved cache line ~~having a first address comprising a first companion bit value~~ with a the companion cache line if the cache line is determined to be compressible;

storing the combined cache line in the cache line of the resident companion; ~~having a second address comprising a second companion bit value if the companion cache line is resident in the cache memory, wherein the second address differs from the first address by the second companion bit~~; and

storing a component of the data in one or more of a plurality of storage pools.

25. (Original) The method of claim 24 wherein the plurality of cache lines are included within a plurality of sets.

26. (Original) The method of claim 25 further comprising allocating a storage pool to each of the plurality of sets.

27. (Original) The method of claim 26 further comprising associating an indicator with each storage field of a storage pool to indicate a line within one of the plurality of sets to which a storage field is assigned.

28. (Original) The method of claim 25 further comprising allocating a storage pool to a line within one of the plurality of sets.

29. (Original) The method of claim 28 further comprising mapping each storage field to one of the plurality of sets.

30. (Original) The method of claim 29 further comprising associating an indicator with each line of a storage pool to indicate which of the plurality of sets to which a storage field is assigned.

31. (Previously Presented) A computer system comprising:

a central processing unit (CPU); and

a cache memory, coupled to the CPU, including:

main cache having a plurality of cache lines, each of the plurality of cache lines being compressible to form compressed cache lines to store additional data; and

a plurality of storage pools to hold a segment of the additional data for a compressed cache line; and

a main memory device coupled to the CPU; and

a cache controller having compression logic to determine that a retrieved cache line is to be combined with a resident companion cache line to form the compressed cache line if the companion cache line is resident in the cache memory and to store the compressed cache line in the cache line of the resident companion ~~form the compressed cache line by combining a retrieved cache line having a first address comprising a first companion bit value with a companion cache line having a second address comprising a second companion bit value if the companion cache line is resident in the cache memory, wherein the second address differs from the first address by the second companion bit~~.

32. (Original) The computer system of claim 31 wherein each of the plurality of storage pools include a plurality of fixed width storage fields.

33. (Original) The computer system of claim 31 wherein the plurality of cache lines are included within a plurality of sets.